VLSI Circuit for Programmable Sorting

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Abstract — A circuit for sorting analog quantities is described, which yields analog representations of sorted values and digital codings of the related ranks. The length of the sorted list can be digitally programmed at run time to support partial sorting. The modular structure facilitates layout design. Suitable coupling current-mode and voltage-mode signals minimizes the number of transistors.

I. Introduction

Research on VLSI implementations of several information-processing methods [1-3] strongly enforces the interest in hardware support of sorting functions. On the other hand, the global information necessarily involved in sorting typically makes this operation difficult to implement in VLSI efficiently [8].

The paper presents a design method for a programmable VLSI realization of sorting functions. The circuit processes a set of N analog input currents, and outputs k sorted voltages proportional to the largest k input values; the circuit can be programmed by digitally setting the desired length, k, of the sorted list. The system completes a sorting cycle in O(k) time.

The principle of operation is straightforward: sorting results from iteratively 1) detecting and consequently 2) inhibiting the highest value in the list. Sorting proceeds sequentially; the inhibiting circuitry is digital, hence a simple counter is needed to control the process.

Maximum-value detection - Detecting the highest value represents a crucial step in the overall system. To single out the largest input current, the well-known Winner-Take-All (WTA) circuit described in [5] is used. The basic WTA circuit is arranged into elementary cells operating at the local level and interacting through a single wire (Fig.1). As a result of a competitive process, the whole sink current Ib flows through the winning cell, whereas all other cells remain switched off.

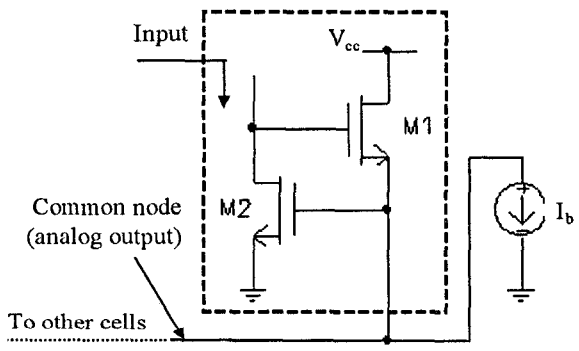

Fig.1 – Elementary cell for WTA maximum-value detection

Linear output - An enhancement of Lazzaro's original circuit makes it possible to attain an analog, voltage-mode representation of the winning value from the potential at the common node [6].

Sequential sorting - The mechanism for progressively inhibiting the largest values exploits the peculiar cur-rent distribution of the WTA circuit. Each cell can locally detect whether it is currently the winner by check-ing the drain current in transistor M1. Such a current is then digitally converted, and drives a switch that dis-connects the entire cell from the rest of the circuit. This removes the largest value from the list, and the sec-ond largest input current will drive a new winning unit. A synchronization clock supplies delays for current redistribution.

II. The Sorting Circuit

The overall schema is arranged into cells operating at the local level. Fig. 2 presents the elementary cell that processes each sorted quantity. Input values are represented in current-mode. Potential Vb forces M6 to pull a drain current equal to the WTA sink current, Ib. The D-flip-flop is triggered by the falling edge of the clock; at initialization, the Reset signal forces Vo(D) to low, hence Mswitch is on.

The transistor couple (M1,M2) reflects Lazzaro's classical schema; node Vo(A) is the cell-connecting node broadcasting the winning potential. As a result, disregarding additional circuitry, the set of cells keeps supporting the WTA behaviour. Thanks to a suitable polarization technique of the input currents [6], potential Vo(A) represents the largest input value linearly.

The transistor set M4, M5, M6 operates as a current comparator [7], matching the local status of the WTA cell against the expected status of a winning cell. As soon as the cell wins the WTA competition, the drain current in M5 will be equal to Ib, and Iwin will drop to zero.

The circuit section M7, M8, M9, M10 converts its input current I_{win} to a digital voltage, V_{win}, which is low when I_{win} is not null. A high-to-low transition of V_{win} occurs in the winning cell and forces a change in the associated flip-flop. The flip-flop status is exported from the cell as a digital output Vo(D), and informs the external circuitry about which cell has won the competition. The position of the winning

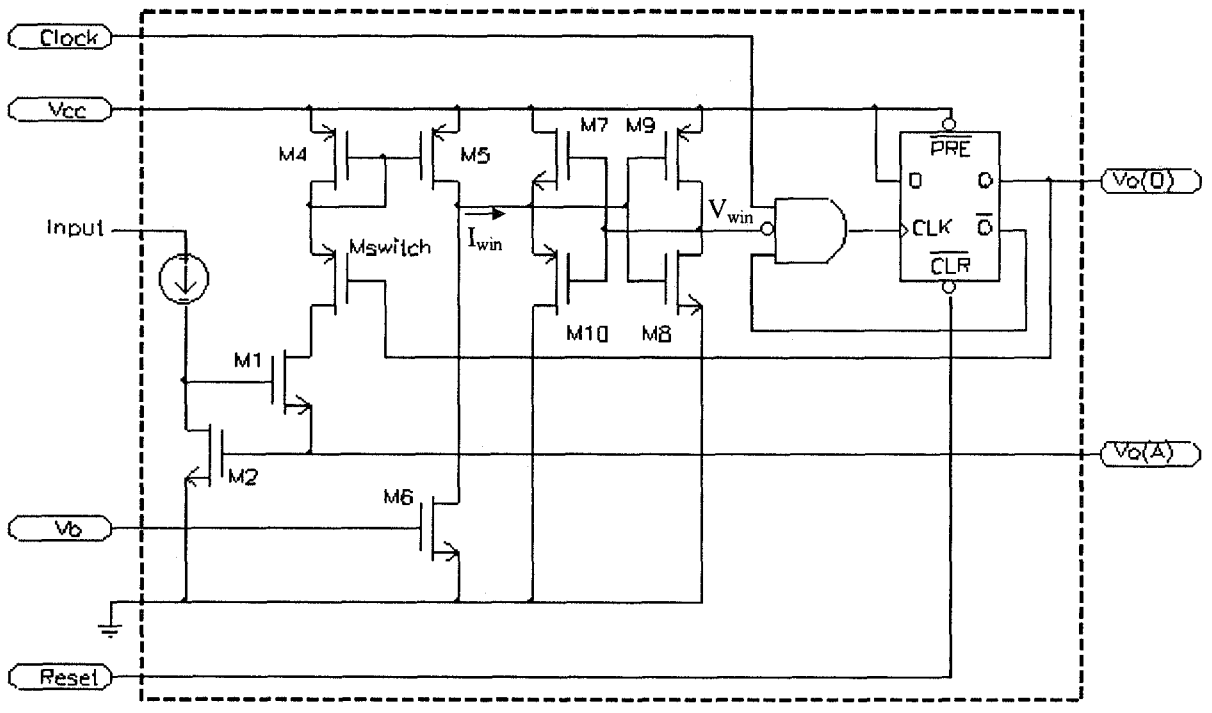

Fig.2 – The elementary cell of the sorting circuit

input in the list can be easily detected by a counter. Voltage Vo(A) outputs an analog representation of the winning input. The flip-flop also controls the internal status of the cell. Further changes in the flip-flop status are inhibited by feeding back its inverted output. Instead, the direct output line, Q, switches off the pass transistor M_{switch}. This disconnects the WTA cell from the others, hence the associated input will not affect the competition any longer (analog feedback).

Therefore, at each iteration, the largest value is first detected and then removed from the list. Sorting will eventually stem from collecting the series of digital outputs and their corresponding analog values.

The length of the sorted list can be controlled by feeding digital output signals to a counter that eventually disables the entire system and resets all cells. The overall sorting circuit simply derives from connecting all analog output lines to a common node as per Fig.1.

The global sorting circuit can be set up by interconnecting the elementary cells associated with each input value through the single wire and setting the digitl control circuit accordingly. The overall circuit architecture is presented in Fig.3.

III. Implementation and Performance

Architecture – The most significant feature of the cell-oriented architecture is its modularity. In the described architecture, one wire connects all cells. This feature is counterbalanced by the system's sequential functioning. The area complexity is simply $O(N)$, as opposed to other analog solutions (such as the Maxnet [9], requiring $O(N^2)$ connections) or digital approaches [4,10], requiring $O(N \log N)$ gates.

In theory, the modular approach makes the number of processed inputs virtually unbounded; in fact, this number is limited by the discrimination accuracy of the WTA structure, by the chip area, and by parasitic capacitances in long connections.

VLSI implementation –The mixed analog/digital approach enhances the internal structure as follows. Section M1, M2 implements the actual analog WTA processing. The accuracy in matching and dimensioning equals that needed for a correct functioning of the elementary WTA subcircuit. Disregarding the tiny pass transistor M_{switch}, section M4, M5, M6 involves a digital, current-mode representation; the wide range of operating conditions for I_{win} greatly enhances robustness. This also holds for the current-to-voltage mapping section M7, M8, M9, M10, whose nonlinear feedback makes up for mismatchings. From a general perspective, mixing current-mode and voltage-mode representations ultimately increases the implementation simplicity.

Timing performances – The settling time of the competitive section is very short, but it is hard to determine analytically due to asynchronous positive and negative feedbacks.

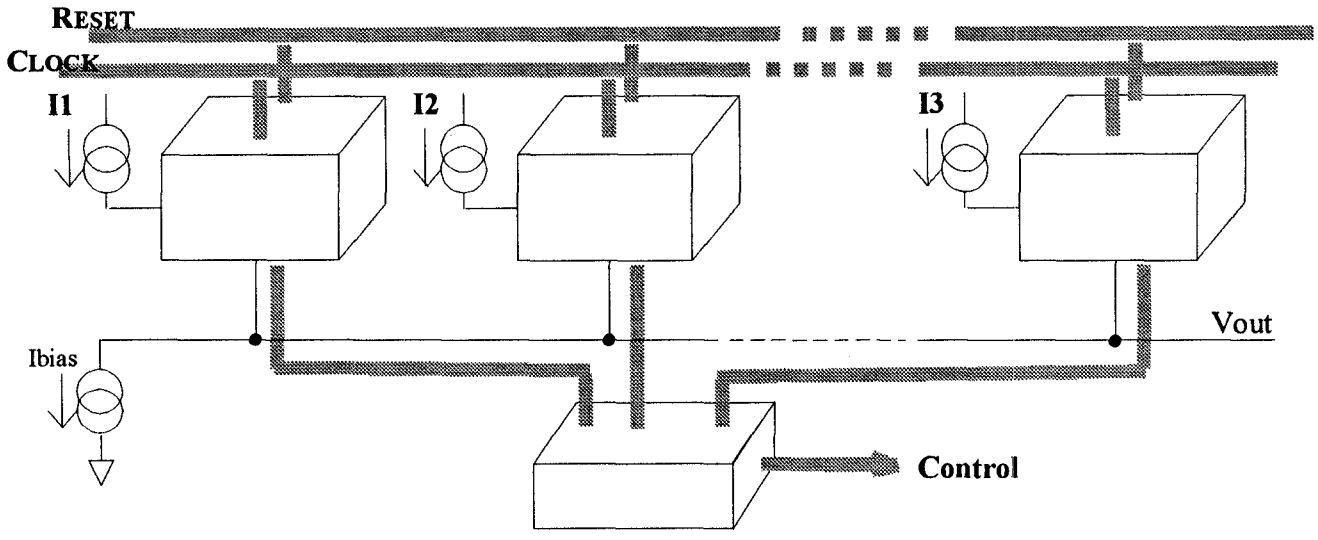

Fig.3 - The global sorting circuit

We implemented a realization with $N=64$. With input signals very close to each other (worst case), a typical settling time for Vo(A) is about 300 ns, corresponding to a clock speed of about 3Mhz (3 000 000/k inputs sorted per second). This results from the netlist extracted from the layout simulator, since the plain schematic-based simulation gives much better results (about 10 times faster). Conversely, Vo(D) requires for settling about 10ns+the propagation delay of the flip-flop; this results in a speed of 100 000 000/k inputs sorted per second.

The time complexity is therefore O(k), a function not of the total number of inputs, but only of the programmed number of sorted elements. This is in contrast with other analog approaches, in which the complex dynamics does not ensure a O(1) time for the maximum selection [9]. There are examples of k-WTA circuits with complexity O(N) in area and O(1) in time [10], but they cannot provide the complete sort function.

IV. RESULTS

The circuit layout has been tested with HSPICE level 13 and 1μm technology. The transistor sizes (W/L) in Fig.2 are as follows: M1,M2: 25/2; Mswitch: 2/2; M4,M5: 5/2; M6:30/2; M7,M9: 6/2; M8,M10: 3/2 – power voltage is 0-5V;

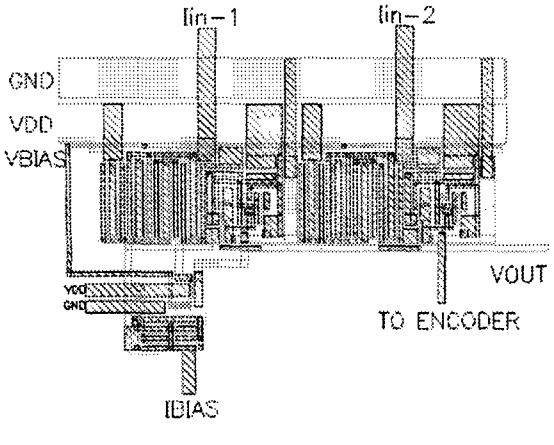

Fig.4 – Layout excerpt of a cell structure

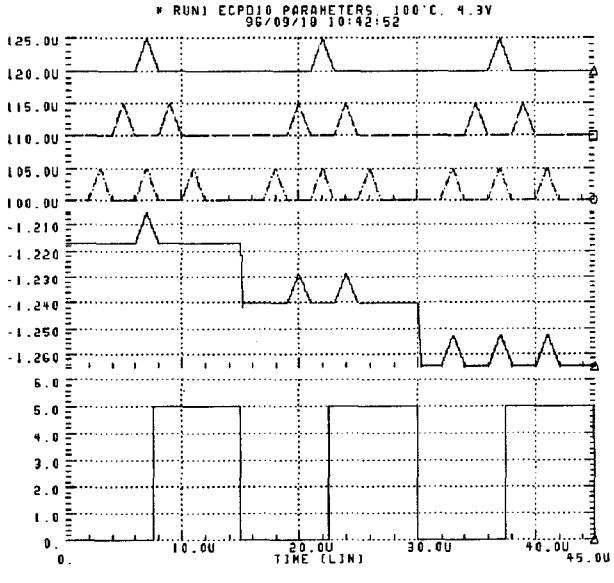

Fig. 5 – SPICE simulation results

Ib=30μA. Fig. 4 displays the layout of a pair of WTA cells.

Experimental tests confirmed the validity of the circuit design.. Fig.5 presents the output of a SPICE simulation, showing the correct functiooning of the sorting circuit; it can be verified that each clock strike (bottom) determines a change in the output analog representation (second from bottom), mapping the correct sequence of input currents (three top panels).

The sorting module is a subpart of a circuit for the VLSI support of vector quantization [11]. The whole chip stores 64 codevectors and processes 64-dimensional patterns (analog inputs and codevetors). Each vector unit evaluates the Euclidean distance from the input pattern, and the WTA/sorting module works out the k best-matching codevectors. The application domain is image coding; layout simulations give an effective operating speed of 2MHz, allowing the chip to attain a frame rate of about 240 frames/sec for standard 512x512, 8bpp images. These results outperform digital VLSI approaches to VQ implementations, which yield maximum frame rates of about 30 frames/sec [12].

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