

MIXED ANALOG-DIGITAL CIRCUIT FOR LINEAR-TIME PROGRAMMABLE SORTING

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Abstract—The paper describes a VLSI circuit for sorting analog quantities. The circuit yields analog representations of sorted values and digitally encodes the corresponding ranks in the list. The length of the sorted list can be digitally programmed at run time, hence partial sortings are also supported. The modular, mixed analog/digital structure is arranged into elementary cells operating at the local level. This greatly facilitates the layout design. A suitable coupling of current-mode and voltage-mode signals minimizes the number of transistors.

I. INTRODUCTION

Sorting represents a basic operation in many information-processing paradigms. For example, pattern recognition [1], neural networks [2], and evolutionary computation models [3] typically require sorting at crucial steps in the training processes. Recent research on VLSI implementations of such approaches strongly enforces the interest in hardware support of sorting functions. On the other hand, the global information necessarily involved in sorting typically makes this operation difficult to implement in VLSI efficiently [8].

This paper presents a design method for a programmable VLSI realization of sorting functions. The circuit processes a set of N analog input currents, and outputs k sorted voltages proportional to the largest k input values; the circuit can be programmed by digitally setting the desired length, k , of the sorted list. The system completes a sorting cycle in $O(k)$ time.

As opposed to our approach, most sorting circuits available in the literature process digital quantities [4]. On the one hand, digital circuits are simpler to design and can be used in a variety of situations. On the other hand, however, the analog modules that we have exploited are very fast, whereas the size and time complexity of the whole system compare favourably with those of other approaches, with the added benefit of a fully modular structure. Finally, one of the main drawbacks of analog signal processors, namely, the lack of flexibility, has been overcome by introducing a programmable structure.

In the rest of the paper, the structure is introduced (Sect. II) and explained in more detail (Sect. III). Then some comments on the architecture are presented (Sect. IV). Sect. V contains some concluding remarks.

II. OVERVIEW

The principle of operation is straightforward: sorting results from iteratively 1) detecting and consequently 2) inhibiting the highest value in the list. Thus sorting proceeds sequentially; the inhibiting circuitry is digital, hence a simple counter is needed to control the process.

Maximum detection - Detecting the highest value represents a crucial step in the overall system. To single out the largest input current, the well-known Winner-Take-All (WTA) circuit described in [5] is used. The basic WTA circuit is arranged into elementary cells operating at the local level and interacting through a single wire (Fig.1). As a result of a competitive process, the whole sink current I_b flows through the winning cell, whereas all other cells remain switched off.

Linear output - An enhancement of Lazzaro's original circuit makes it possible to linearize the output characteristic and to attain an analog, voltage-mode representation of the winning value from the potential at the common node [6].

Sequential sorting - The mechanism for progressively inhibiting the largest values exploits the peculiar current distribution of the WTA circuit. Each cell can locally detect whether it is currently the winner by checking the drain current in transistor M1. Such a current is then converted into a digital signal and used to drive a switch that disconnects the entire cell from the rest of the circuit. This virtually removes the largest value from the list, and the second largest input current will drive a new winning unit. A synchroniza-

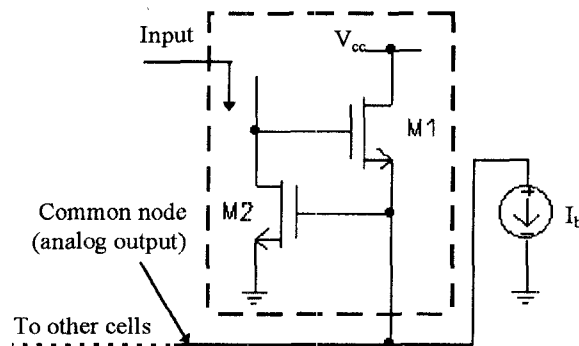


Fig.1 - WTA cell [5] for max detection

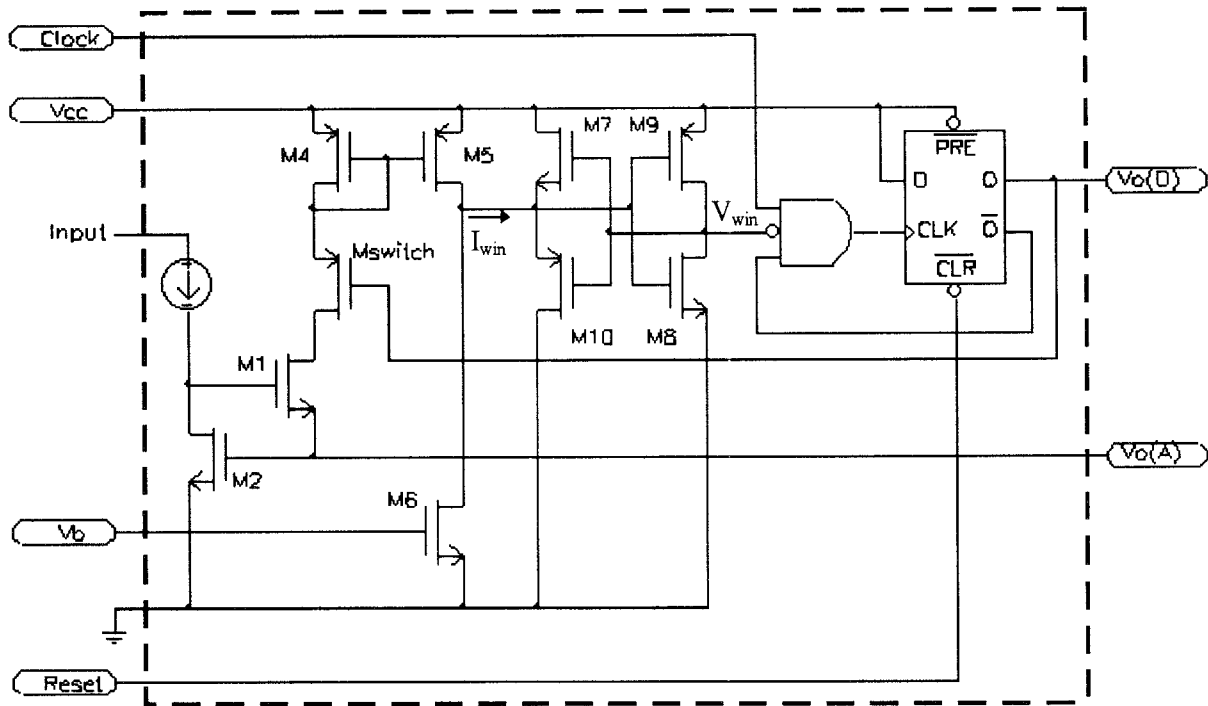


Fig.2 - Elementary cell of the sorting circuit

tion clock supplies delays for current redistribution. In summary, potential readings at the output analog node will show up in a decreasing ordered sequence. The process can be stopped by simply counting the number of extracted values; the total timing for this sequential sorting will be proportional to the number of elements extracted.

III. THE SORTING CIRCUIT

This section describes the functioning of the sorting circuitry in detail. The overall schema is arranged into cells operating at the local level. Figure 2 presents the structure of the elementary cell that processes each sorted quantity. Input values are represented in current-mode. Potential V_b forces M6 to pull a drain current equal to the WTA sink current, I_b . The D-flip-flop is triggered by the falling edge of the clock; at initialization, the Reset signal forces $V_o(D)$ to low, hence M_{switch} is on.

The transistor couple (M1,M2) reflects Lazzaro's classical schema; node $V_o(A)$ is the cell-connecting node broadcasting the winning potential. As a result, disregarding additional circuitry, the set of cells keeps supporting the WTA behaviour. Thanks to a suitable polarization technique of the input currents [6], potential $V_o(A)$ represents the largest input value linearly.

The transistor set M4, M5, M6 operates as a current comparator, matching the local status of the WTA

cell against the expected status of a winning cell. As soon as the cell wins the WTA competition, the drain current in M5 will be equal to I_b , and I_{win} will drop to zero.

The circuit section M7, M8, M9, M10 converts its input current I_{win} to a digital voltage [7], V_{win} , which is low when I_{win} is not null. As a consequence, a high-to-low transition of V_{win} occurs in the winning cell and forces a change in the associated flip-flop status.

The flip-flop status is exported from the cell as a digital output $V_o(D)$, and informs the external circuitry about which cell has won the competition. The position of the winning input in the list can be easily detected by a counter. Voltage $V_o(A)$ outputs an analog representation of the actual winning input.

The flip-flop output also controls the internal status of the cell. Further changes in the flip-flop status are inhibited by feeding back its inverted output, \bar{Q} (digital feedback). Instead, the direct output line, Q , switches off the pass transistor M_{switch} . This disconnects the WTA cell from the others, hence the associated input will not affect the competition any longer (analog feedback).

The global result of this operation is that, at each iteration, the largest value is first detected and then automatically removed from the list. Sorting will eventually stem from collecting the series of digital outputs and their corresponding analog values.

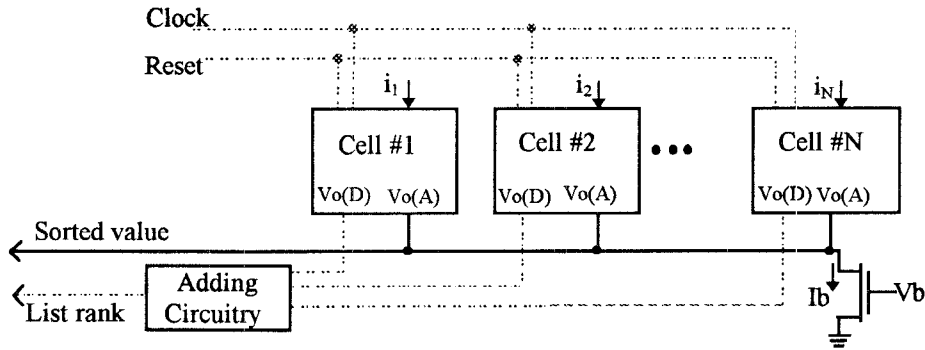


Fig.3 - The global sorting circuit - Dashed lines indicate digital signals

The length of the sorted list can be controlled by feeding digital signals to a counter that eventually disables the entire system and resets all cells. The schema of the overall sorting circuit is given in Fig.3, where cell interconnections are shown.

IV. IMPLEMENTATION AND PERFORMANCE ISSUES

Architecture – The most significant feature of the cell-oriented architecture is its modularity. Other implementation approaches to the sorting problem require a huge amount of unit interconnections [8]. In the described architecture, one wire connects all cells, which operate at the local level. This feature is counterbalanced by the system’s sequential functioning. The area complexity is simply $O(N)$, as opposed to other analog solutions (such as the Maxnet [9], requiring $O(N^2)$ connections) or digital approaches [4], requiring $O(N \log N)$ gates.

In theory, the modular approach makes the number of processed inputs virtually unbounded; in fact, this number is limited by the discrimination accuracy of the WTA structure, by the chip area, and by parasitic capacitances in long connections.

VLSI implementation – The mixed analog/digital approach enhances the internal structure as follows. Section M1, M2 implements the actual analog WTA processing. This is the system’s most sensitive subpart; the accuracy in matching and dimensioning equals that needed for a correct functioning of the elementary WTA subcircuit. Disregarding the tiny pass transistor M_{switch} , section M4, M5, M6 involves a digital, current-mode representation; the wide range of operating conditions for I_{win} greatly enhances implementation robustness. This also holds for the current-to-voltage mapping section M7, M8, M9, M10, whose nonlinear feedback makes up for mismatches. In practice, with a careful design the NOT gate on this line and the digital feed-back can be removed: this approach, however, might also affect the overall implementation robustness by tightening precision constraints. From a

general perspective, mixing current-mode and voltage-mode representations ultimately increases the implementation simplicity.

Timing performances – The settling time of the competitive section is very short, but it is hard to determine analytically since the WTA structure is based on asynchronous positive and negative feedbacks. Experimentally, the settling time depends on many factors: number of inputs, layout (parasitic capacitances), and heavily on the quantity read as output. If we need to read the sequence of ordered levels, $V_o(A)$, it is necessary to wait for the oscillations in the output voltage to be sufficiently small. If we read the ordered input positions, $V_o(D)$, the only quantities involved in the competitive process are currents, which do not oscillate at all.

As a reference, we take a realization with $N=64$. With input signals very close to each other (worst case), a typical settling time for $V_o(A)$ is about 300 ns, corresponding to a clock speed of about 3Mhz (3 000 000/ k inputs sorted per second). This results from the netlist extracted from the layout simulator, since the plain schematic-based simulation gives much better results (about 10 times faster). Conversely, $V_o(D)$ requires for settling about 10ns + the propagation delay of the flip-flop; this results in a speed of 100 000 000/ k inputs sorted per second.

The time complexity is therefore $O(k)$, a function not of the total number of inputs, but only of the programmed number of sorted elements. This is in contrast with other analog approaches, in which the complex dynamics does not ensure a $O(1)$ time for the maximum selection [9]. There are examples of k -WTA circuits with complexity $O(N)$ in area and $O(1)$ in time [10], but they cannot provide the complete sort function.

V. IMPLEMENTATION RESULTS AND DISCUSSION

The circuit layout has been tested with HSPICE level 13 and $1\mu\text{m}$ technology. The transistor sizes (W/L) in Fig.2 are as follows: M1,M2: 25/2; Mswitch: 2/2;

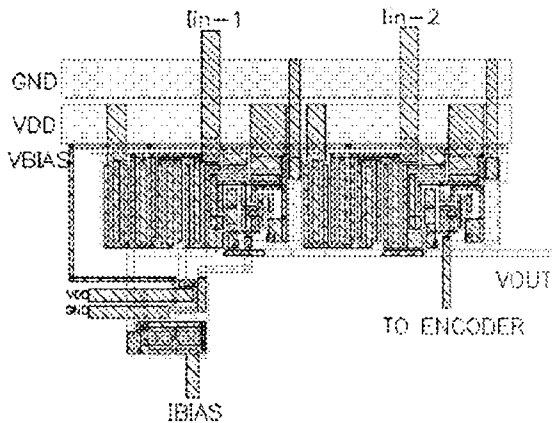


Fig.4 - Layout of two WTA cells

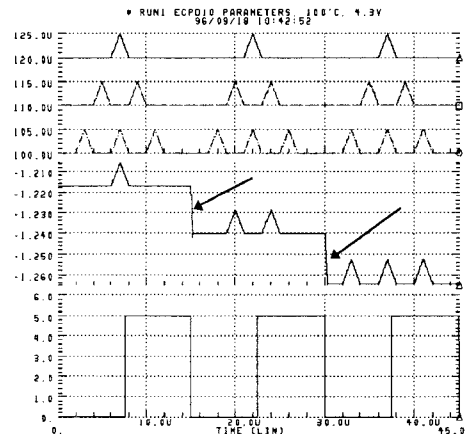


Fig.5 - Run-time sorting result

M4,M5: 5/2; M6:30/2; M7,M9: 6/2; M8,M10: 3/2 – power voltage is 0-5V; $I_b=30\mu A$. Figure 4 displays the layout of a pair of WTA cells.

Experimental tests confirmed the validity of the circuit design. In Figure 5, an excerpt from an actual HSPICE printout shows three steps of the system's sorting process. The upper section displays three current inputs with base values of 100, 110, and 120 μA , respectively. In the middle section, the output analog voltage is plotted; the clock is shown at the bottom. At $t=0$, input one prevails and is remapped to the output. The arrows point out two subsequent (clock-triggered) eliminations of the previous winners, hence inputs i_2 and i_3 , respectively, are mapped to the output.

The sorting module is a subpart of a circuit for the VLSI support of vector quantization tools [11]. The whole chip stores 64 codevectors and processes 64-dimensional patterns (analog inputs and codevectors). Each vector unit evaluates the Euclidean distance from the input pattern, and the WTA/sorting module works out the k best-matching codevectors. The application domain is image coding; layout simulations give an effective operating speed of 2MHz, allowing the chip to attain a frame rate of about 240 frames/sec for standard 512x512, 8bpp images. These results outperform digital VLSI approaches to VQ system implementations, which attain maximum frame rates of about 30 frames/sec [12].

Future lines of research in this area will include the actual chip production and field testing. Parallel research will concentrate on the development of an integrated environment of VQ-based image coding including additional modules for adaptive coding and quad-tree support.

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