

FLEXIBLE VIDEO COMPRESSION SYSTEMS USING AN ANALOG VECTOR QUANTIZATION CHIP

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ABSTRACT

Vector quantization systems are usually based on digital implementation of the core operations. In this paper, video compression systems exploiting an analog implementation of vector quantization are presented. The main advantages of analog design are exploited, obtaining notable performances when compared to other solutions found in the literature. The circuit features a very modular, completely parallel internal architecture. Many circuits can be easily connected to obtain a larger codebook size and a larger vector dimension. Synthesis of codebooks is also described.

1. INTRODUCTION

Vector quantization (VQ) is a lossy compression technique that has gained interest in recent times for video applications. We observe that the need for efficient image compression systems is increasing as the number and scope of image-oriented applicative areas grows. Lossy compression techniques have received great emphasis, and ISO and CCITT compression standards for both moving and still images (CCITT H261/H263, the ISO MPEG family, JPEG...) are based on such approach. Another feature that may be requested is the ability to perform real-time decompression.

Among these techniques, VQ features a unique mix of simplicity in the decoding phase and good compression ratios obtainable for the mid-quality range, qualifying as perhaps the best candidate in very low bit rate applications. These features account for the notable development of VQ techniques in past years [1]. This paper outlines a number of system configurations exploiting an analog VLSI vector quantization chip.

VQ algorithms are structurally simple. However, they require a time-consuming sweep of the whole codebook; therefore they are ideal candidates for concurrent implementations. It is possible to devise a highly parallel system, based on simple independent operators, that features $O(1)$ search time: the number of vectors in the codebook and the dimension of vectors (size of image blocks) have no influence on retrieval performance (of course, a price is paid in terms of area, since the number of processors is proportional to codebook size). Moreover, the parallel structure allows building modular, multi-chip systems that can be expanded with the simple addition of new blocks, without modifying the existing circuit.

Analog implementation allows the high density of operations required. Digital elements are adopted in sections of the circuit that would not benefit of an analog implementation.

In the literature, VQ implementation is usually addressed by fully digital approaches, often aiming at maximum speed for real-time video processing [2][3], but in some cases also at expandability [4]. Analog realizations can be found especially in the neural network field [5]. The main strength of the analog approach is that some functions, even complex, do not require an algorithmic formulation, but can be implemented in a quite simple circuit configuration. Examples are given by summation of current signals, which requires a simple node, and exponentiation of voltage signals, provided directly by a P-N junction.

2. IMPLEMENTING VECTOR QUANTIZATION IN ANALOG VLSI

The fundamental functions of a VQ system [1] are outlined as follows. At the sender's end of the transmission channel is the encoder. Its task is to read the input vector and to select, from a given codebook of uniquely labeled reference vectors, the best-matching codevector. Typically the label is simply an integer index, for accessing a lookup table that implements the codebook. The index is then transmitted on the channel, and used at the receiver's end to address a local copy of the same lookup table. The output of the system is given by the best matching codevector thus retrieved.

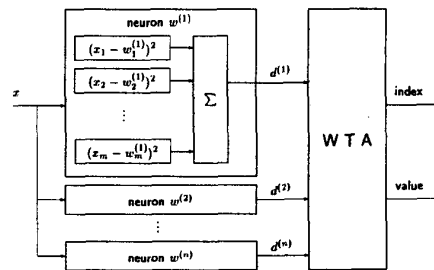


Figure 1. Block diagram of a generic nearest neighbor encoder for vector quantization.

Usual VQ implementations rely on optimizing the codebook-search algorithm to attain desired performances. In contrast to algorithm-based digital implementations, an analog implementation can be based on massively parallel operations, without requiring complicated control functions. This makes it possible to implement a constant-time codebook search.

Figure 1 shows the functions required to implement an Euclidean nearest-neighbor encoder. Each codevector $w(k)$ corresponds to a subsystem that computes the Euclidean distance $d(k)$ between the codevector (which is stored permanently) and the input vector. The Euclidean distance is a sum of squared differences. The subsequent block is the competition circuit, for selecting the best-matching codevector given an input vector. The best match corresponds to the lowest distance. This block is often termed a "winner-take-all" (WTA) network [7]. The output of the WTA block is a pointer to the winning neuron, in 1-out-of- n encoding, which can be translated (by means of a digital encoder) into an integer index and finally transmitted.

3. THE VQ CHIP

The chip presented has the following structure. A single codevector is implemented by a subsystem which stores its components locally in as many capacitors as input lines, and includes a circuit that computes its Euclidean distance from the input vector. The square of difference operation is also implemented for each input component. A special purpose multiplier (Figure 2) has been designed to minimize the number of components, exploiting the fact that the square operation is a two-quadrant multiplication.

The distance values obtained are compared with a circuit block for detection of the minimum, derived from enhancements of a standard scheme [7]. This block, shown in Figure 3, selects the minimum instead of maximum. Moreover, it features two outputs: the usual index of the winning input, and the corresponding input value. This is used to implement modular systems and to enable use in codebook adaptation systems. These applications will be outlined in the following section.

The necessary refresh circuitry for the analog memory uses an external digital memory (a standard RAM) and a bank of D/A

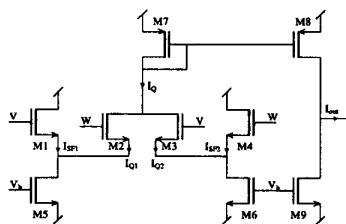


Figure 2. Circuit that computes the square of a difference.

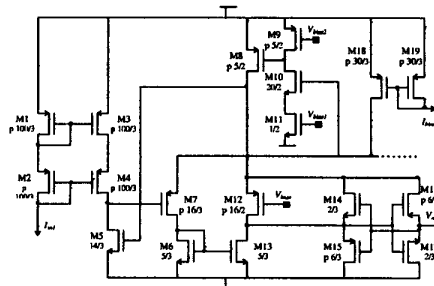


Figure 3. Circuit for the competition and selection of minimum distance..

converters. Analog memories are accessed with binary row/column addresses. Analog multiplexing has apparent drawbacks, however it is necessary because of the huge number of analog memories to be accessed.

The chip has been developed using the ECPD10 $1\mu\text{m}$ technology, provided by the Europractice service. The range for input voltages is 1V, and the corresponding signals have 7-bit precision. A photograph of the circuit is presented in Figure 5.

The project is based on blocks of size 8×8 , yielding a vector dimension of 64. There are 64 codevectors in a chip. Therefore there are 4096 square-of-difference circuits and as many analog memories, whereas the competition block has 64 inputs.

For experimental purposes, the circuit has been realized in a reduced configuration. Since the area was constrained to about $4 \times 4 \text{ mm}^2$, to allow realistic experiments the vector dimension was reduced to 16 (4×4 blocks), instead of greatly reducing only codebook size. Therefore the realized chip contains 40 codevectors with dimension 16.

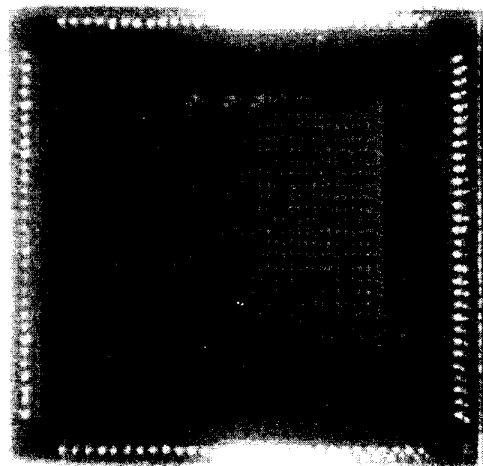


Figure 4. Photograph of the chip.

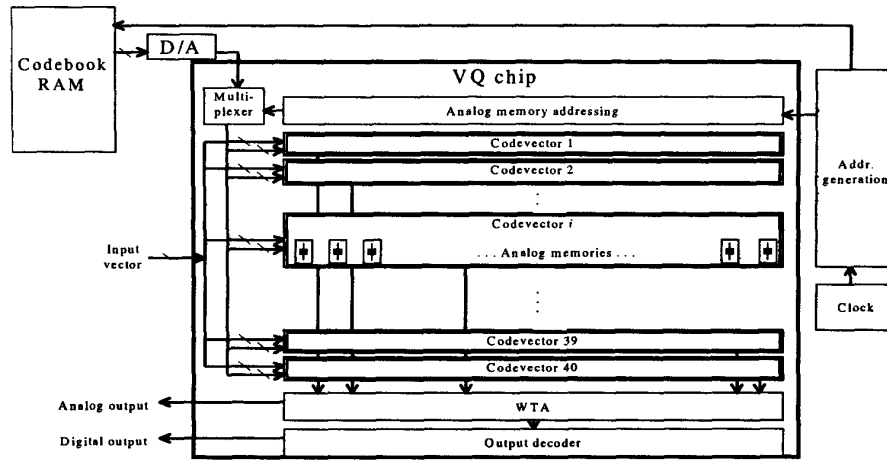


Figure 5. Block diagram of a basic VQ encoder.

The features of the circuit are summarized as follows: the vector density is 40 vector components per mm²; the circuit has an average power consumption of about 0.5W and an analog storage precision of more than 7bit. Throughput is about 1000k vectors/s, equivalent to a frame rate (for 640x480 pixel frames) of 100 frames/s.

An outline of a complete VQ system, including the chip and external components, is presented in the block diagram of Figure 5.

4. VIDEO CODING SYSTEM DESIGN USING THE ANALOG VQ CHIP

In this section, the use and configuration of the presented chip as a component for compact video systems is described.

The external circuitry is simple enough to be realizable in integrated form. A multi-chip-module solution is possible as well, resulting in a very compact system (suitable for instance for set-top box video systems).

A control system for the presented chip should incorporate the digital memory for codebook storage, the codebook D/A converters, and control circuitry to generate refresh sequences and to provide external synchronization.

One of the goals of the circuit presented is to provide easy expandability and flexibility. Both codebook size and vector dimension can be adapted without redesigning the circuit, but simply by appropriately connecting several chips. An auxiliary chip is required to establish the connection among chips. This auxiliary component is simply a stand-alone version of the competition stage (WTA).

Codebook size can be increased by splitting the overall codebook into several portions, each maintained by a dedicated chip. The supplementary competition stage selects the final

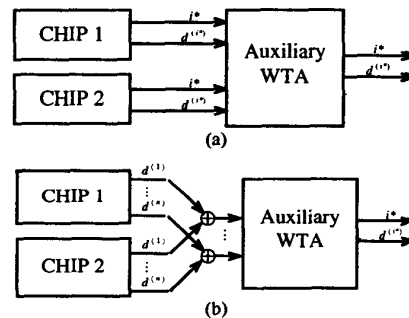


Figure 6. (a) VQ system with a connection to increase codebook size. (b) VQ system with a connection to increase vector dimension.

winning distance among the values present on the analog outputs of each chip. The address in the codebook is then formed by the index of the winning circuit, and by the index of the winning codevector within its circuit (two digital words, adjoined so that the circuit index is in the most significant position). This connection is sketched in Figure 6(a).

Increasing vector dimension requires external availability of all distance values. Since Euclidean distance is a sum of partial distances for each vector space component, by using n chips, each dealing with a subset of the components of the vectors, the total distance can be obtained by summing the partial distances obtained from each chip. To this purpose, the distance of all codevectors is made available as an output (as previously stated). The external competition circuit implements the final selection. This connection is sketched in Figure 6(b).

Figure 7 sketches a complete, multiple video encoding system with image format of 160x120 pixels. A codebook with size 64 and block size 4x4 is assumed; therefore, 2 VQ chips are required, connected as in Figure 6a. We can estimate a "raw" compression ratio (before channel encoding) of about 20 (it could be increased by increasing block size). The frame rate with the format specified is constrained only by the bandwidth, since the processors are capable of processing about 800 frames/sec. Therefore, a high level of multiplexing is possible.

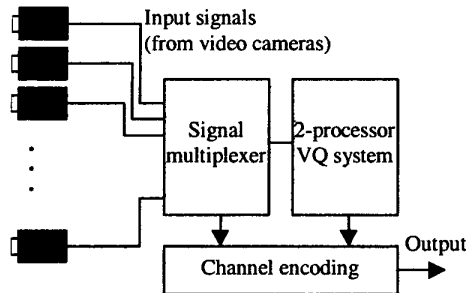


Figure 7. Block diagram of a complete video encoding system.

Adaptation of codebooks can be obtained by adding suitable circuitry to implement a vector quantization training procedure. This is again made possible by the availability of the winner's distance at the output, since all codebook adaptation algorithms require this value (computed on the vectors of a training set) for updating the codebook.

Synthesis of codebooks is an important step in vector quantization design. Therefore, the choice of a good algorithm is often a central task. Availability of the necessary signals make it reasonably easy to apply most usual techniques and some more exotic algorithms, such as those found in the neural network field.

Figure 8 shows a codebook adaptation system based on the analog VQ processor.

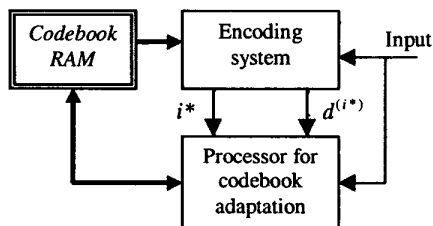


Figure 8. Block diagram of a codebook adaptation system.

5. CONCLUSION AND FUTURE WORK

In this paper, video coding systems employing vector quantization have been presented. The designs are based on an analog VQ chip designed to compare favorably with the far more common digital implementations found in the literature. The main strength of the circuit is the flexibility obtained by a modular design and by appropriate selection of input/output signals and signal format.

Further work on this project will be based on integration of the support circuitry required to operate the VQ chip. The auxiliary competition block and the control/memory/conversion functions will be included in two chips, forming a complete chipset for video systems.

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