Initialization

$init \longrightarrow pinit(p,l)$

$pinit(p,l) \longrightarrow pinit(p',l') \mid linit(r,k) \;\; : \; p' > p, l' = l, r = p, k = l$

$linit(p,l) \longrightarrow invalid(q,m) \mid linit(p',l') \;\; : \; p = q, l = m, p' = p, l' > l$

Read Miss

$$\begin{array}{lll} invalid(p,l) & \longrightarrow valid(p',l') & \\ \;\;[\; dirty(q,k) & \hookrightarrow \; valid(q',k') & : \; p' = p, l' = l, q \neq p, k = l, k' = k, l = m, r \neq p, r' = r, m' = m \\ \;\;\;\; exclusive(r,m) & \hookrightarrow \; valid(r',m') \;] & \end{array}$$

Write Miss

$$\begin{array}{lll} invalid(p,l) & \longrightarrow exclusive(p',l') & \\ \;\;[\; dirty(q,k) & \hookrightarrow \; invalid(q',k'), & \\ \;\;\;\; valid(r,j) & \hookrightarrow \; invalid(r',j') & : \; p' = p, l' = l, q \neq p, k = l, k' = k, r \neq p, r' = r, j = l, j' = j, s \neq p, l = m, s' = s, m' = m \\ \;\;\;\; exclusive(s,m) & \hookrightarrow \; invalid(s',m') \;] & \end{array}$$

$exclusive(p,l) \longrightarrow dirty(p',l') \;\; : \; p' = p, l' = l$

Write Hit

$$\begin{array}{lll} valid(p,l) & \longrightarrow exclusive(p',l') & \\ \;\;[\; dirty(q,k) & \hookrightarrow \; invalid(q',k'), & \\ \;\;\;\; valid(r,j) & \hookrightarrow \; invalid(r',j') & : \; p' = p, l' = l, q \neq p, k = l, k' = k, r \neq p, r' = r, j = l, j' = j, s \neq p, l = m, s' = s, m' = m \\ \;\;\;\; exclusive(s,m) & \hookrightarrow \; invalid(s',m') \;] & \end{array}$$

Read/Write Hit

$valid(p,l) \longrightarrow valid(p',l') \;\; : \; p' = p, l' = l$

$exclusive(p,l) \longrightarrow exclusive(p',l') \;\; : \; p' = p, l' = l$

$dirty(p,l) \longrightarrow dirty(p',l') \;\; : \; p' = p, l' = l$

Eviction

$valid(p,l) \longrightarrow invalid(p',l') \;\; : \; p' = p, l' = l$

$shared(p,l) \longrightarrow invalid(p',l') \;\; : \; p' = p, l' = l$

Fig. 3. Specification of the M.S.I. cache coherence protocol